

DATA SHEET

74HC3G07; 74HCT3G07 Buffer with open-drain outputs

Product specification

2003 Oct 15

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- High noise immunity
- Low power dissipation
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74HC3G/HCT3G07 is a high-speed Si-gate CMOS device. Specified in compliance with JEDEC standard no. 7A.

The 74HC3G/HCT3G07 provides three non-inverting buffers.

The outputs of the 74HC3G/HCT3G07 devices are open drains and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC3G	HCT3G	
t_{PZL}	propagation delay nA to nY	$C_L = 50$ pF; $V_{CC} = 4.5$ V	9	11	ns
t_{PLZ}	propagation delay nA to nY	$C_L = 50$ pF; $V_{CC} = 4.5$ V	11	10	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	4	4	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. For 74HC3G07 the condition is $V_I = \text{GND}$ to V_{CC} .

For 74HCT3G07 the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5$ V.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	L
H	Z

Note

- H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC3G07DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H07
74HCT3G07DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T07
74HC3G07DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H07
74HCT3G07DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	T07

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	3Y	data output
3	2A	data input
4	GND	ground (0 V)
5	2Y	data output
6	3A	data input
7	1Y	data output
8	V _{CC}	supply voltage

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

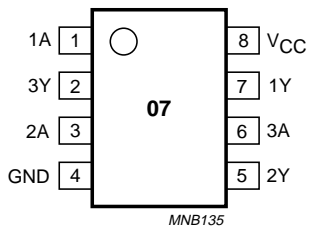


Fig.1 Pin configuration.

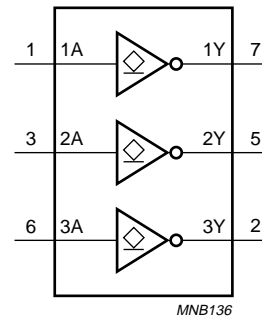


Fig.2 Logic symbol.

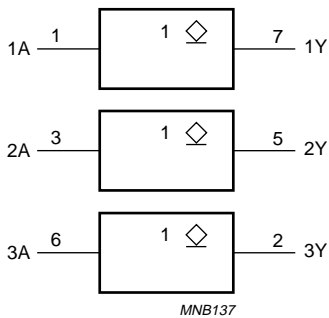


Fig.3 IEC logic symbol.

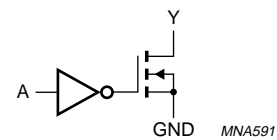


Fig.4 Logic diagram (one driver).

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC3G07			74HCT3G07			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	6.0	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5$ V	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0$ V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V	–	–20	mA
V_O	output voltage	active mode; note 1	–0.5	$V_{CC} + 0.5$	V
		high-impedance mode; note 1	–0.5	7.0	V
I_O	output sink current	-0.5 V < V_O < 7.0 V	–	–25	mA
I_{CC}	V_{CC} or GND current	note 1	–	50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

DC CHARACTERISTICS

Type 74HC3G07

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	0	0.1	V
		I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 20 µA	6.0	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
		I _O = 5.2 mA	6.0	–	0.16	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	10	µA
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	–	0.1	V
		I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 20 µA	6.0	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
		I _O = 5.2 mA	6.0	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	20	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

Type 74HCT3G07

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	10	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	375	µA
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	410	µA

Note1. All typical values are measured at T_{amb} = 25 °C.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

AC CHARACTERISTICS

Type 74HC3G07

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	25	95	ns
			4.5	–	9	19	ns
			6.0	–	7	16	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	25	95	ns
			4.5	–	11	23	ns
			6.0	–	10	23	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	18	95	ns
			4.5	–	6	19	ns
			6.0	–	5	16	ns
T_{amb} = -40 to +125 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	30	ns
			6.0	–	–	26	ns
t _{THL}	output transition time	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

Type 74HCT3G07GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

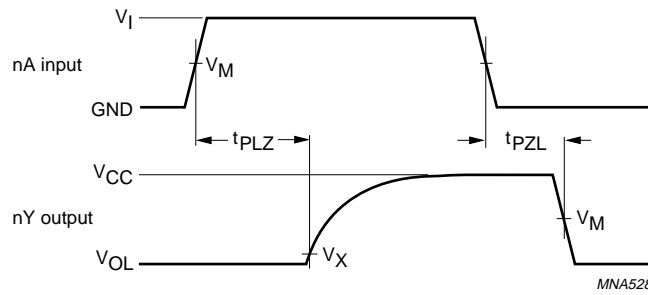
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	4.5	–	11	27	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	4.5	–	10	26	ns
t _{THL}	output transition time	see Figs 5 and 6	4.5	–	6	19	ns
T_{amb} = -40 to +125 °C							
t _{PZL}	propagation delay nA to nY	see Figs 5 and 6	4.5	–	–	32	ns
t _{PLZ}	propagation delay nA to nY	see Figs 5 and 6	4.5	–	–	31	ns
t _{THL}	output transition time	see Figs 5 and 6	4.5	–	–	22	ns

Note1. All typical values are measured at T_{amb} = 25 °C.

Buffer with open-drain outputs

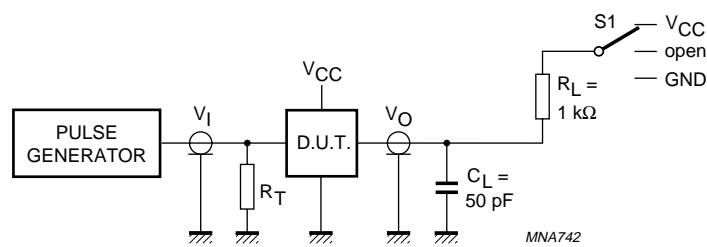
74HC3G07; 74HCT3G07

AC WAVEFORMS



For 74HC3G07: $V_M = 50\%$; $V_1 = \text{GND to } V_{CC}$.
 For 74HCT3G07: $V_M = 1.3 \text{ V}$; $V_1 = \text{GND to } 3.0 \text{ V}$.
 For 74HC3G07 and 74HCT3G07: $V_x = 0.1 \times V_{CC}$.

Fig.5 The input (nA) to output (nY) propagation delays and transition times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 R_L = Load resistor.
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

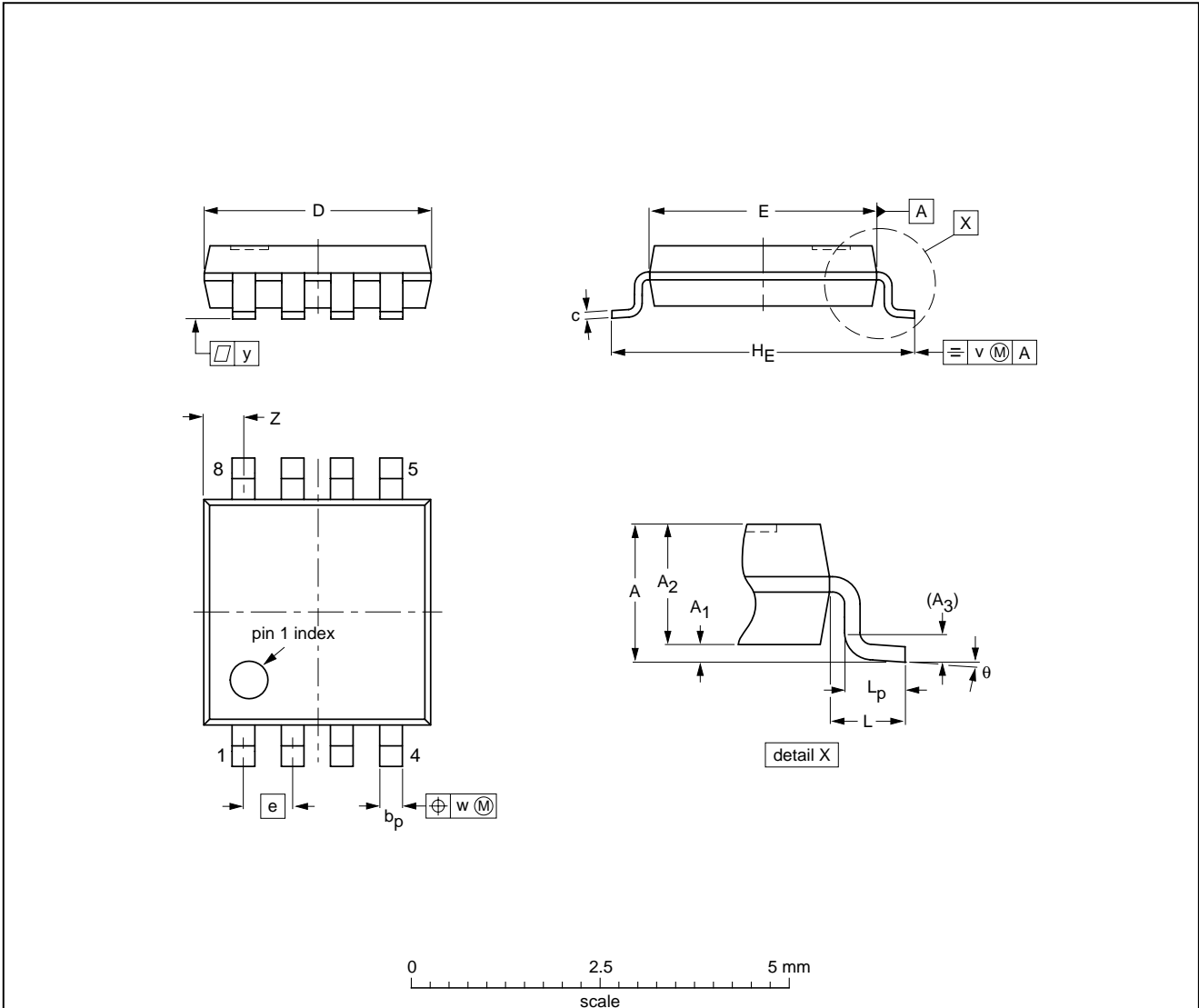
Fig.6 Load circuitry for switching times.

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

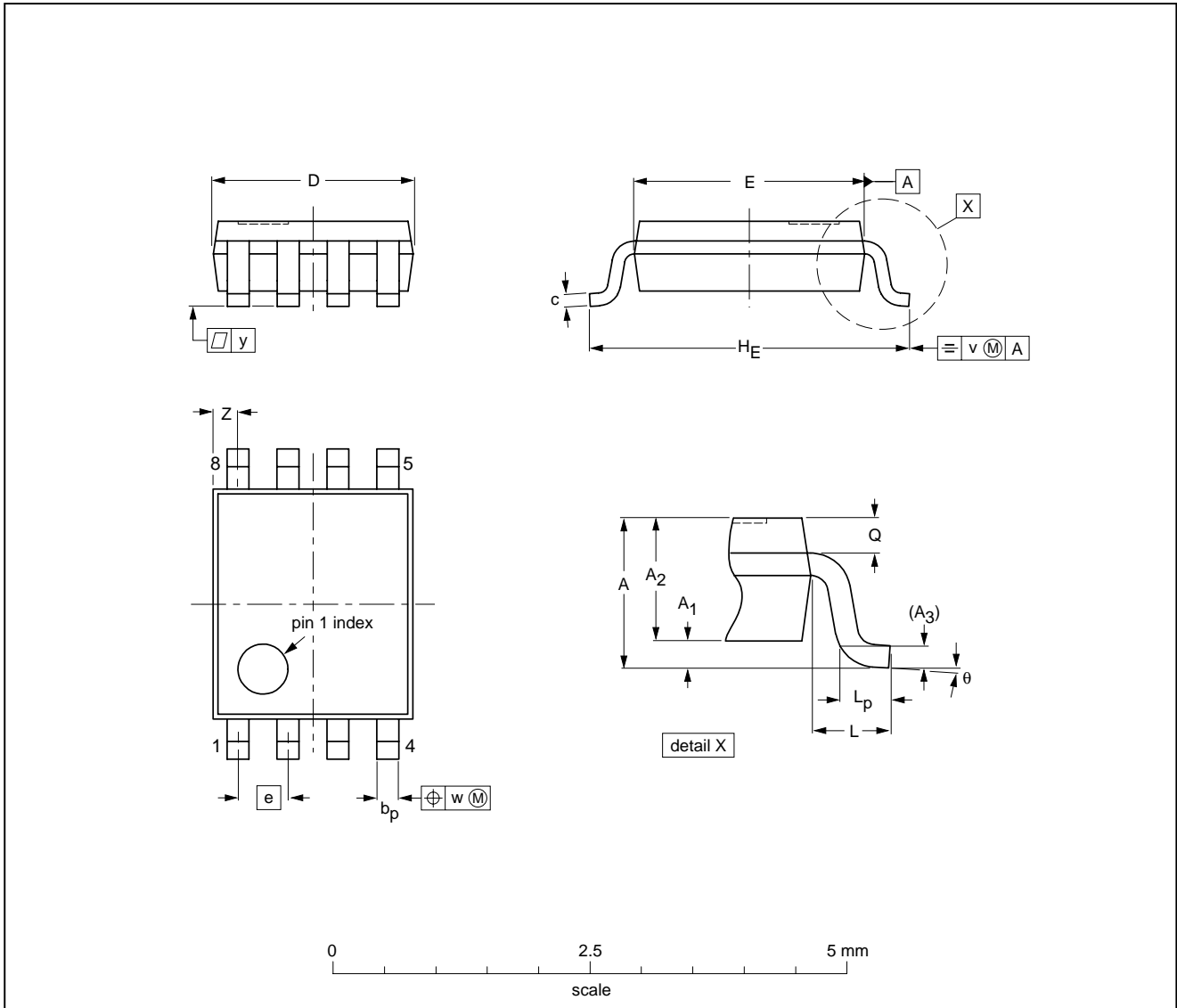
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT505-2		---			02-01-16

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Buffer with open-drain outputs

74HC3G07; 74HCT3G07

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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